IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

THE TRUSTEES OF PURDUE UNIVERSITY, Plaintiff, vs. STMICROELECTRONICS N.V., ET AL, Defendants.	6:21–CV–727-ADA JURY TRIAL DEMANDED

RESPONDING DECLARATION OF VIVEK SUBRAMANIAN, PH.D.

I, Dr. Vivek Subramanian declare as follows:

I. INTRODUCTION

1. I submit this Responding Declaration concerning technical subject matter relevant to claim construction for U.S. Patent Nos. 7,498,633 ("the '633 Patent") and 8,035,112 ("the '112 Patent"). The facts and opinions stated in this declaration are true and of my own personal knowledge or investigation and as an expert in this field. If called to testify, I could and would testify to these facts and opinions, and any other facts that I become aware of after the filing of this declaration.

2. I incorporate by reference my opening declaration signed February 22, 2022.

3. I have reviewed the responding claim construction brief provide by Purdue and the supporting materials attached to it, including the declaration of Ishwara Bhat, Ph.D.

II. SUMMARY OF OPINIONS

a. A POSITA and the Technology at Issue

4. Purdue and Dr. Bhat make two arguments. First they argue that I do not satisfy the standard for being a POSITA under Purdue's narrowed definition. And second, they argue that the proposed standard for a POSITA in this case requires specific experience designing silicon carbide MOSFETs. I disagree with both assertions.

5. Purdue and Dr. Bhat argue that my background and experience do not meet Purdue's definition for a POSITA for the inventions of the asserted claims on the basis that design of silicon carbide devices present considerations at the detail level that are different than silicon. I disagree. First, silicon is just one type of semiconductor material among many types of semiconductor materials. And silicon carbide is just one type of wide bandgap semiconductor material among the many types of wide bandgap semiconductors (e.g., zinc oxide and indium oxide). Further, silicon carbide MOSFETs are just one type of wide bandgap device. Therefore, my experience with the design of semiconductor devices does not, as Purdue and Dr. Bhat state, mean experience only with silicon. Additionally, Purdue incorrectly states that "none of the publications and patents listed on [Dr. Subramanian's] CV relate to wide bandgap devices." That is not correct. I have researched and published numerous papers on wide bandgap devices over more than a decade.

6. Purdue and Dr. Bhat next argue that my definition of a POSITA is incorrect, and that the correct definition requires a POSITA to have experience with silicon carbide MOSFETs. I disagree. Dr. Bhat makes many comments about the experience and education of a POSITA and what a POSITA would know based on specific details about how silicon carbide devices are said to be different than silicon devices. *See, e.g.*, ¶¶ 15-23 and declaration generally. I believe that

most of these comments go far beyond the scope of the claims at issue and, therefore, are out of context. They do not address what a POSITA would know and conclude about the disputed claim terms at the level of detail of the claims and disclosure of the patents. For that reason, I respond generally and do not respond to many of the individual comments for reasons that will be apparent in the following paragraphs.

7. Dr. Bhat discusses many specific characteristics of silicon carbide versus silicon that may be considered in a specific design, addressing detailed topics such as on-resistance and blocking voltage (*see* ¶ 16), resistive elements including silicon carbide drift region resistance (*see* ¶ 18), maximum electric field in the oxide under the gate (*see* ¶ 19), maximum JFET width (*see* ¶ 20), and channel resistance versus drift-region resistance (*see* ¶ 21) and concludes "[a]s such, a SiC MOSFET and a silicon MOSFET have completely different design considerations, owing to the fundamental differences in their respective material properties." (*see* ¶ 21). However, the specification and the prosecution history of the '633 Patent teach that the disclosed invention and general configuration of claim 9, including several of the limitations added to secure allowance, are not presented as uniquely and specifically directed to silicon carbide devices. And except for JFET width in the '633 Patent, none of the claims at issue specify any of the parameters identified in Dr. Bhat's declaration noted above.

8. Instead, the specification of the '633 Patent is generic with regard to the type of substate material and most of the original application claims, including the claims with limitations on JFET gap size were not limited to silicon carbide devices. The specification describes that "The semiconductor substrate ***may be*** formed from a silicon carbide material." '633 Patent at 1:44-45 (added emphasis). And the specification repeatedly indicates that silicon carbide is only an example of a substrate material. *Id*. at 2:31-32; 3:7-9; 4:11-12; 4:39-40. Originally filed

application claim 12 (now claim 9) contained the disputed limitation that "the JFET region having a width less than about three micrometers" yet neither original claim 12 nor any original claim depending from claim 12 required a silicon carbide substrate. *See* original claims filed with the application for the '633 Patent attached as Exhibit 1. The same is true for original application claims 3, 4, 6, 13, and 20, which also address the width of the JFET region but do not limit the claims to a device with a silicon carbide substrate. *Id*. Thus, the basic configuration of original claim 12 (now claim 9) including the limitation of "the JFET region having a width less than about three micrometers" is not presented in the '633 Patent and prosecution history as specific to a device with a silicon carbide substrate.

9. Similarly, application claim 12 was amended during prosecution to add specific requirements about the shape and position of source and base contact regions, but these limitations are not taught in the patent as specific or unique to silicon carbide. For example, original application claims 10, 11, 15, 16, and 21 all variously recite limitations about the shape and position of source and base contact regions and none of these original claims are limited to silicon carbide. *See* Exhibit 1. In fact, issued claim 12 (application claim 17) of the '633 Patent includes limitations regarding the shape and position of source and base contact regions (i.e., formed in alternating strips) yet issued claim 12 does not include a limitation of a silicon carbide substrate. *Id*. Thus, the general configuration of the claims including the limitations relating to the configuration of the source and base contact regions were not presented in the '633 Patent as specifically unique to silicon carbide.

10. Likewise, the specification of the '112 Patent repeatedly emphasizes that the invention focuses on a "self-aligned contact." *See e.g.*, '112 Patent at Title; 1:21-23; 2:24-26; 5:23-25; 6:66-7:2. The contact layer is formed above the substate and the various matters

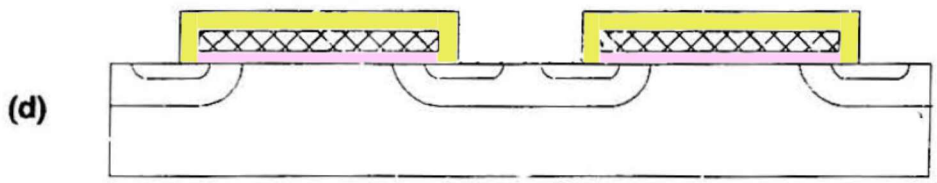
addressed in Dr. Bhat's declaration such as on-resistance and blocking voltage (*see* ¶ 16), resistive elements including silicon carbide drift region resistance (*see* ¶ 18), maximum electric field in the oxide under the gate (*see* ¶ 19), maximum JFET width (*see* ¶ 20), and channel resistance versus drift-region resistance (*see* ¶ 21) do not address the contact layer. The '112 Patent notes that silicon carbide oxidizes more quickly than polysilicon and the patent "tak[es] advantage" of this, but Dr. Bhat ignores this point and Purdue argues that it would be improper to limit the oxide layer over the gates to the type of oxide formed by growing. However, the alternative to growing an oxide is depositing an oxide and when a deposited oxide is used, the composition of the substate (whether silicon or silicon carbide) is not at issue. As a result, the various specific design matters addressed in Dr. Bhat's declaration such as on-resistance and blocking voltage (¶ 16), resistive elements including silicon carbide drift region resistance (¶ 18), maximum electric field in the oxide under the gate (¶ 19), maximum JFET width (¶ 20), and channel resistance versus drift-region resistance (¶ 21) are off subject with respect to disputed oxide layer terms of the invention of the '112 Patent. Regardless, the ability to form insulating layers such as oxides by oxidation as well as by deposition are within the knowledge and experience of a POSITA as I have explained one. Accordingly, it's my opinion that Purdue and Dr. Bhat are incorrect when they argue that a POSITA for the '633 and '112 Patents must have training or experience that is specific to silicon-carbide semiconductor devices. Instead, a person with general semiconductor experience would know that different semiconductor materials have different characteristics, for example bandgap, and that the design of a device would need to take the characteristics in to account.

b. Deposited Versus Grown Oxide

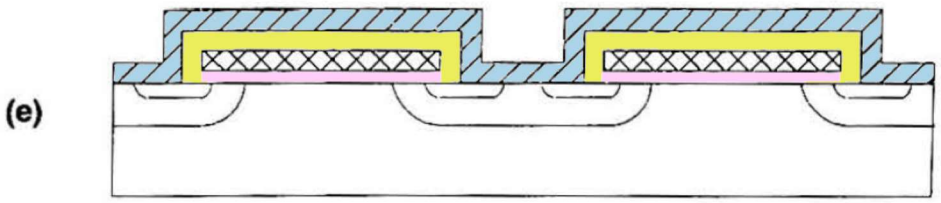
11. In my opening declaration I note the different steps involved between depositing an oxide and growing and oxide and the necessity to use a photomask to create an opening in a

deposited oxide for a later deposited source electrode. The specification of the '112 Patent also discloses this difference. The '112 Patent incorporates by reference a textbook by B. Jayant Baliga. *See* '112 Patent at 1:45-49. The Baliga book describes a conventional process in making a power MOSFET in which the gates are covered with a ***deposited*** oxide so that a source electrode can later be deposited as a layer over the whole structure without contacting the gates. *See* Baliga at 410-12; Fig. 7.53. Baliga describes that after individual gates are formed and N+ regions are formed (Fig. 7.53(c)), "a thick layer of oxide is deposited by using low pressure chemical vapor deposition (LPCVD). This provides a conformal insulating film over the top and sides of the polysilicon gate electrode." *Id*. at 412. A POSITA would recognize that Baliga expressly describes this layer as one that is "deposited." Regardless, a POSITA would also recognize that a low pressure chemical vapor deposition (LPCVD) of an oxide layer is a deposited layer, not a layer grown by oxidizing the gate and substrate surfaces. Baliga continues and explains, "The oxide layer is now patterned to form the contact windows as illustrated in Fig. 7.53(d)."

12. A POSITA would understand that "patterned to form the contact windows" means that a photomask step is performed to create the openings (i.e., "windows") through the deposited oxide layer in select areas because the deposited oxide upon being deposited would cover the entire device with a layer of substantially uniform thickness. As shown in Fig. 7.53(d) the patterned oxide (highlighted in yellow below) covers the tops and sides of the gates (cross-hatched) with the window openings in the oxide having been formed by pattering, leaving exposed the surface areas of the substrate between the gates (source and base contact regions).



13. Baliga explains, "The final step in the device process consists of metallization to create the structure shown in Fig. 7.53(e)." As shown in Fig. 7.53(e), the top of the device is covered with metal, which a POSITA would understand to be the "metallization" referred to by Baliga, so that the metal goes across the device and into the openings (i.e., windows) created through the deposited oxide and makes contact with the substrate surface and source and base contact regions exposed there.



14. As a result, the Baliga material incorporated by reference into the specification of the '112 Patent provides a side-by-side comparison of one manufacturing option that ***deposits*** an oxide layer over the gates, which then requires a patterning step using a mask as described immediately above (Baliga 410-412; Fig. 7.53), versus the alternative of growing an oxide layer where the grown oxide is used to avoid the necessity of using a mask step to form the openings through the oxide layer to expose the substrate and N+ and + implants there ('112 Patent at 5:61-6:50).

15. Baliga explains the risk of using a deposited oxide layer and patterning with a mask step:

> "The oxide layer is now patterned to form the contact windows as illustrated in Fig. 7.53(d). This is another critical photolithographic step in the DMOS process because misalignment can either cause poor contact to the P-base region or lead to an overlap of the contact with the polysilicon at the cell edges. This overlap will produce a short between source and gate." *Id*. at 412.

c. Preamble of claim 9 of the ’633 Patent

16. The Bhat Declaration asserts that “a POSITA would know that Claim 9 of the ’633 Patent refers to a DMOSFET in silicon carbide even without an explicit statement to that effect … in light of the claim language, the specification and the drawings” (*see* ¶ 28) and that from the body of the claim a POSITA would understand it to be a MOSFET. (*see* ¶ 30) However, saying that a POSITA would understand this from the “specification and the drawings” appears to be reading in select limitations from the specification rather than focusing on the claim language. Indeed, the specification suggests that other types of devices are within the scope. For example, the specification says “Referring to FIG. 1, a high-voltage power semiconductor device 10 includes a substrate 12 and a number of semiconductor layers successionally formed on the substrate 12. Illustratively, the semiconductor device 10 is a vertical double implanted metal-oxide semiconductor field-effect transistor (DMOSFET). However, in other embodiments, the semiconductor device 10 may be embodied as other types of MOSFET devices.” ’633 Patent at 4:4-11. Likewise, the specification says “While the disclosure has been illustrated and described in detail in the drawings and foregoing description, such an illustration and description is to be considered as exemplary and not restrictive in character, it being understood that only illustrative embodiments have been shown and described and that all changes and modifications that come within the spirit of the disclosure are desired to be protected.” *Id.* at 8:38-44.

a. Less than about 3 micrometers

17. The Bhat Declaration also asserts that a “POSITA would reasonably understand that ‘about,’ when referring to numerical values such as in the ’633 Patent generally implies ±10% variation” (*see* ¶ 31) and that “a POSITA would know that the JFET width after fabrication cannot be specified to exact values, but rather a distribution with range and standard deviation.” (*see* ¶

32) However, as explained in my opening declaration and addressed further in the following, there is nothing in the patent or prosecution history to indicate what objective is intended with respect to the JFET width limitation.

18. The Bhat Declaration asserts that a POSITA would know that a 3µm JFET width is optimum for silicon carbide and would recognize that capturing values close to the optimum width is the purpose of the JFET width limitation in the claim. *See* ¶¶ 32-36 and declaration generally. However, as I have already noted, the limitation of "the JFET region having a width less than about three micrometers" is not presented in the '633 Patent or prosecution history as specific to a device with a silicon carbide substrate. Because the specification and original claims do not limit to silicon carbide, I do not agree that a POSITA reviewing the patent, prosecution history and the asserted claim would conclude that the purpose of the 3µm limitation is directed to the theoretically optimum JFET gap for silicon carbide. Indeed, issued claim 15 of the '633 Patent includes a limitation similar to that in claim 9 that "the JFET region has a width of about three micrometers or less," yet claim 15 is not limited to silicon carbide. Further, given the range of JFET width recited in claim 9, which purports to encompass all possible JFET widths less than about 3µm, the claim itself is contrary to the thesis that the purpose of the 3µm limitation relates to the theoretically optimum JFET gap for silicon carbide because the claim covers a wide range of non-optimum JFET widths.

19. The Bhat Declaration also refers to an Exhibit C for support for the proposition that 3um JFET with is optimal. *See* ¶ 36, citing "Sei-Hyung Ryu, Anant K. Agarwal, Nelson S. Saks, Mrinal K. Das, Lori A. Lipkin, Ranbir Singh & John W. Palmour, "Design and Process Issues for Silicon Carbide Power DiMOSFETS," in Mat. Res. Soc. Symp. Vol. 640, pp. H4.5.1 – H.4.5.6 (2001) (evaluating 2-5 micrometer JFET width and concluding three micrometers is optimal).)

However, the Bhat Declaration fails to note that 3µm JFET gap in that article was determined as "optimal for 2000V 4H-SiC DiMOSFET with 25 µm thick, $3x10^{-15}cm^{-3}$ doped drift layer." *See* Bhat Declaration Exhibit C at p H.4.5.6 (ST-PURDUE_00007891). In contrast, asserted claim 9 does not specify any voltages, thicknesses, or doping concentrations.

20. The same article that the Bhat Declaration cites in ¶ 36 also notes that while it determined a 3µm JFET gap was optimal (for the particular design characteristics) "However, JFET gap of 5 µm was used to account for implant straggles and other process biases." Bhat Declaration Exhibit C at p. H.4.5.2 (ST-PURDUE_00007887). Increasing the design specification from a calculated 3µm optimal JFET gap to 5µm to account for "implant straggles and other process biases" (a 66.7% increase) is inconsistent with the Bhat Declaration where it states that a dimension such as the 3 micrometer JFET gap would be understood to be +/- 10% to account for these very same manufacturing issues. *See* ¶¶ 31-32 where the Bhat Declaration specifically refers to "transverse (or lateral) straggle of the ion-implantation species" as one basis for "uncertainty in the measurement of precise values in the manufactured devices."

21. The Bhat Declaration also contends that "POSITA would understand that the goal of the device design is to achieve the lowest possible on-resistance while still meeting the desired blocking voltage specification." *See* ¶ 34. However, the claim is not limited to a device with the lowest possible on-resistance or with any particular desired blocking voltage specification. The asserted claim addresses a structure with a single dimension (JFET width) required, albeit with indefinite precision. To require the claim be limited to designs that would be optimum or even commercially practical would be to read in limitations not addressed in the claim or the specification.

22. The Bhat Declaration also states that "the lower bound for JFET width is limited by the manufacturing process technology. The '633 Patent gives an example of 'about one micrometer.'" *See* ¶ 36. The specification of the '633 Patent does mention "the JFET may have a width of about one micrometer" (1:66-67; 2:48-49) but the patent does not say or suggest that this dimension relates to the limit of manufacturing process technology. Further, the material cited in the Bhat Declaration shows that $R_{on,sp}$ increases dramatically below a JFET width of one micrometer (*See* ¶ 35), which would negatively affect device performance. Further, paragraph 35 of the Bhat Declaration includes a graph but does not reproduce the caption which recites the particular details of the device graphed. The caption is shown below (see Bhat Declaration Exhibit B at p. 2782 - ST-PURDUE_00003135):

Fig. 2. Variations of V_B, $R_{ON,SP}$, and $V_B^2/R_{ON,SP}$ with JFET width. In this comparison, $N_{epi} = 1E16$ cm^{-3}, $N_{CSL} = 1E17$ cm^{-3}, $N_J = 5E16$ cm^{-3}; L_P, L_S, L_{GS}, and L_{GO} are 2 μm each, and $L_{CH} = 0.5$ μm.

23. The omitted caption shows that the data is based on a device with specific characteristics: N_{epi} = 1E16 cm^{-3}, N_{CSL} = 1E17 cm^{-3}, N_J=5E16 cm^{-3}; L_P, L_S, L_{GS}, and L_{GO} are 2µm each, and L_{CH} = 0.5µm. In contrast, the asserted claim does not specify any of these types of characteristics.

24. I reserve the right to supplement my opinions in the future to respond to any arguments that Purdue raises and to take into account new information as it becomes available to me. I also reserve the right to provide additional opinions related to other case issues.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Dated: March 28, 2022

Vivek Subramanian

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Vivek Subramanian